



Call for papers
for a Joint Special Issue of
IEEE Transactions on Electron Devices and
IEEE Transactions on Nanotechnology
on
“Nanowire Electronics”

The rapid development in integrated circuit technology is primarily due to MOSFET downscaling trends that have so far continued to the present day. However, silicon based MOS technology is expected to face fundamental limits in the near future. Therefore, new types of nanoscale devices are being investigated aggressively. The nanowire transistor is one such candidate which has gained significant attention from both device and circuit developers because of its potential for building highly dense and high performance electronic products. Nanowire transistors can be made using different materials on low cost substrates such as glass or plastic. Si and Ge nanowire transistors are of particular importance because of their compatibility with CMOS technology. There are recent publications on MOSFETs using top-down nanowires (e.g. fabricated by conventional lithography and RIE) touting impressive characteristics.

Bottom-up nanowires, on the other hand, have the capability of integrating very dissimilar materials (e.g. InP/InAs or Ge/Si) without generating defects that are typical of two-dimensional (2D) film integration. Nanowires provide a unique opportunity in the direction of heterogeneous devices, especially in silicon where lattice matched systems (such as GaAs/AlGaAs) do not exist. Due to their all-around gate configuration and hence efficient gate control, nanowire transistors (based on either bottom-up or top-down approaches) may become an effective replacement for not only MOSFETs in analog/RF, digital logic, and memory but also in many other applications (e.g. large-area electronics, replacements for current thin-film transistor approaches, chemical/bio-sensors, etc.).

However, control and positioning of nanowires on a chip require expensive tools making it essential to develop self-assembly techniques to reduce the fabrication costs and increase the throughput. Also, nanowire transistors suffer from relatively low on/off ratios and this needs to be overcome using improved device design and appropriate materials. Use of different gate dielectrics and the formation of source/drain regions in nanowire transistors need to be studied carefully for optimal performance of these transistors. In addition, for circuit analysis of nanowire transistors in different applications, simple and efficient compact models need to be developed. Regardless of whether or not nanowire transistors become a commercial technology, there are some important insights that will be relevant to future CMOS device scaling.

There is a diversity of research efforts taking place in applying nanowires for building better electronic systems. The main goal of this joint special issue is therefore to bring together researchers to share their recent results on different aspects of nanowire electronics in order to inspire innovative thinking leading to creative ideas. Suggested topics include, but are not limited to:

1. **Devices:** Nanowire transistors based on silicon, germanium, SiC, ZnO, InP, GaN, other III-V compounds, conducting polymers etc.,
2. **Modeling and Quantum simulations:** Electrical transport properties, performance assessment, compact modeling for circuit design.
3. **Technology:** Top-down and bottom-up fabrication approaches, electrical characterization, contacts, gate dielectrics, vertical structures, glass/plastic substrates and impact of process variations.
4. **Applications:** Analog/RF, digital circuits, memories, large area electronics, sensors, etc.

Submission instructions: Manuscripts should be submitted in a double column format using an IEEE style file. Please visit <http://www.ieee.org/web/publications/authors/transjnl/> to download the templates. In your cover letter, please indicate that your submission is for this joint special issue.

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